What is claimed is:

1. A method for transferring data between an RGB color space memory and a YCrCb color space memory useful for presentation to a DCT block-computation engine, the method comprising:

providing at least two YCrCb intermediate buffers for storing data being transferred between the color space memories; and

using the DCT block-computation engine to access data in one of the YCrCb intermediate buffers while using the other of the YCrCb intermediate buffers for data accesses of the RGB color space memory.

2. The method of claim 1, further including providing at least two RGB intermediate buffers for storing data being transferred between at least one of the YCrCb intermediate buffers and the RGB color space memory.

3. The method of claim 1, further including converting data between the RGB color space memory and the YCrCb color space memory block by block.

4. The method of claim 1, further including converting data between the RGB color space memory and the YCrCb color space memory line by line.

5. The method of claim 1, further including converting data between the RGB color space memory and the YCrCb color space memory word by word.

6. The method of claim 1, wherein the RGB data for a DCT in the YCrCb color space memory is four eight by eight Y arrays, one eight by eight Cr array and one eight by eight Cb array.

7. The method of claim 1, further including compressing the transferred data in the YCrCb color space memory.

8. The method of claim 1, further including decompressing the data in the YCrCb color space memory before using the DCT block-computation engine to access data stored in one of the YCrCb intermediate buffers.

9. A method for transferring data from an RGB color space memory to a YCrCb color space memory in a form useful for presentation to a DCT block-computation engine, the method comprising:

accessing the RBG color space memory and, in response, asynchronously writing RBG values to at least two YCrCb intermediate buffers so that one of the YCrCb intermediate buffers is prepared for use by the DCT block-computation engine before the other of the YCrCb intermediate buffers; and

using the DCT block-computation engine to process data in said one of the YCrCb intermediate buffers while the other of the YCrCb intermediate buffers is storing additional RGB values from the RGB color space memory.

10. A method for transferring data from a YCrCb color space memory to an RGB color space memory, the YCrCb color space memory being in a form useful for access by a DCT block-computation engine, the method comprising:

accessing the YCrCb color space memory and, in response, asynchronously writing YCrCb values to at least two YCrCb intermediate buffers so that one of the YCrCb intermediate buffers is prepared for the RGB color space memory before the other of the YCrCb intermediate buffers; and

reading the YCrCb values from said one of the YCrCb intermediate buffers and writing corresponding RGB values to the RGB color space memory while the other of the YCrCb intermediate buffers is being prepared for the RGB color space memory.

11. A circuit arrangement for transferring data between an RGB color space memory and a YCrCb color space memory useful for presentation to a DCT block-computation engine, comprising:

at least two YCrCb intermediate buffers adapted for storing data being transferred between the color space memories; and

means for using the DCT block-computation engine to access data in one of the YCrCb intermediate buffers while using the other of the YCrCb intermediate buffers for data accesses of the RGB color space memory.

12. An arrangement for transferring data from an RGB color space memory to a YCrCb color space memory in a form useful for presentation to a DCT block-computation engine, comprising:

a DCT block-computation engine;

means for accessing the RBG color space memory and, in response, asynchronously writing RBG values to at least two YCrCb intermediate buffers so that one of the YCrCb intermediate buffers is prepared for use by the DCT block-computation engine before the other of the YCrCb intermediate buffers; and

means for presenting data to the DCT block-computation engine from said one of the YCrCb intermediate buffers while the other of the YCrCb intermediate buffers is storing additional RGB values from the RGB color space memory.

13. The circuit arrangement of claim 12, further including means for converting data in the RGB color space memory to the YCrCb color space memory block by block.

14. The circuit arrangement of claim 12, further including means for converting data in the RGB color space memory to the YCrCb color space memory line by line.

15. The circuit arrangement of claim 12, further including means for converting data in the RGB color space memory to the YCrCb color space memory using word by word.

16. An arrangement for transferring data from a YCrCb color space memory to an RGB color space memory, the YCrCb color space memory being in a form useful for access by a DCT block-computation engine, the method comprising:

means for accessing the YCrCb color space memory and, in response, asynchronously writing YCrCb values to at least two YCrCb intermediate buffers so that one of the YCrCb intermediate buffers is prepared for the RGB color space memory before the other of the YCrCb intermediate buffers; and

means for reading the YCrCb values from said one of the YCrCb intermediate buffers and writing corresponding RGB values to the RGB color space memory while the other of the YCrCb intermediate buffers is being prepared for the RGB color space memory.

17. A circuit arrangement for transferring data between an RGB color space memory and a YCrCb color space memory useful for presentation to a DCT block-computation engine, comprising:

a DCT block-computation engine;

at least two YCrCb intermediate buffers for storing data being transferred between the color space memories; and

logic circuitry adapted to communicate data between the DCT block-computation engine data and one of the YCrCb intermediate buffers while using the other of the YCrCb intermediate buffers for data accesses of the RGB color space memory.

18. The circuit arrangement of claim 17, further including a processor programmed to convert data in the RGB color space memory to the YCrCb color space memory block by block.

19. The circuit arrangement of claim 17, further including a processor programmed to convert data in the RGB color space memory to the YCrCb color space memory line by line.

20. The circuit arrangement of claim 17, further including a processor programmed to convert data in the RGB color space memory to the YCrCb color space memory using word by word.

21. The circuit arrangement of claim 17, further including an RGB intermediate buffer for storing data being transferred between at least one of the YCrCb intermediate buffers and the RGB color space memory.

22. The circuit arrangement of claim 17, further including a second RGB intermediate buffer for storing data being transferred between at least one of the YCrCb intermediate buffers and the RGB color space memory.

23. The circuit arrangement of claim 17, further including an SDRAM configured and arranged to present RGB values from the RGB color space memory to the YCrCb intermediate buffers in multi-byte bursts.

24. The circuit arrangement of claim 17, further including an SDRAM configured and arranged to present RGB values from the RGB color space memory to the YCrCb intermediate buffers in multi-byte bursts.

25. The circuit arrangement of claim 17, wherein said at least two YCrCb intermediate buffers for storing data being transferred between the color space memories includes a Y intermediate buffer, a Cr intermediate buffer, and a Cb intermediate buffer.

26. The circuit arrangement of claim 17, wherein the logic circuitry includes an address calculator adapted to generate selected addresses for RGB values in the RGB color space memory, the selected addresses for the RGB values corresponding to noncontiguous memory locations in the RGB color space memory.

27. An arrangement for transferring data from an RGB color space memory to a YCrCb color space memory in a form useful for presentation to a DCT block-computation engine, the method comprising:

a DCT block-computation engine;

logic circuitry configured and arranged for accessing the RBG color space memory and, in response, asynchronously writing RBG values to at least two YCrCb intermediate buffers so that one of the YCrCb intermediate buffers is prepared for use by the DCT block-computation engine before the other of the YCrCb intermediate buffers; and

a programmed processor circuit adapted to present to the DCT block-computation engine data in said one of the YCrCb intermediate buffers while the other of the YCrCb intermediate buffers is storing additional RGB values from the RGB color space memory.

28. The circuit arrangement of claim 27, wherein the data is presented by transferring the data from the RGB color space block by block.

29. The circuit arrangement of claim 27, wherein the data is presented by transferring the data from the RGB color space line by line.

30. The circuit arrangement of claim 27, wherein the data is presented by transferring the data from the RGB color space word by word.

31. An arrangement for transferring data from a YCrCb color space memory to an RGB color space memory, the YCrCb color space memory being in a form useful for access by a DCT block-computation engine, the method comprising:

at least two YCrCb intermediate buffers;

means for accessing the YCrCb color space memory and, in response, asynchronously writing YCrCb values to said at least two YCrCb intermediate buffers so that one of the YCrCb intermediate buffers is prepared for the RGB color space memory before the other of the YCrCb intermediate buffers; and

means for reading the YCrCb values from said one of the YCrCb intermediate buffers and writing corresponding RGB values to the RGB color space memory while the other of the YCrCb intermediate buffers is being prepared for the RGB color space memory.